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CLOCK GATED POWER SUPPLY NOISE COMPENSATION

CROSS REFERENCE TO RELATED APPLICATION

[0001] The present invention is related to U.S. Application Serial No. _____ (Attorney Docket No. YOR20030363US1) entitled "BUILT IN SELF TEST FOR MEASURING TOTAL TIMING UNCERTAINTY IN A DIGITAL DATA PATH" to Robert L. Franch et al., filed coincident herewith and assigned to the assignee of the present invention.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention is related to integrated circuit (IC) design systems and more particularly to characterizing timing uncertainties in ICs.

Background Description

[0003] Large high performance very large scale integration (VLSI) chips like microprocessors are synchronized to an internal clock. A typical internal clock is distributed throughout the chip, triggering chip registers to synchronously capture incoming data at the register latches and launch data from register latches. Ideally, each clock edge arrives simultaneously at each register every cycle and data arrives at the register latches sufficiently in advance of the respective clock edge, that all registers latch the correct data and simultaneously. Unfortunately, various chip differences can cause timing uncertainty, i.e., a variation in edge arrival to different registers.

[0004] Such timing uncertainties can arise from data propagation variations and/or from clock arrival variations. Data propagation variations, for example, may result in a capturing latch that randomly enters metastability or latches invalid data because the data

may or may not arrive at its input with sufficient set up time. Clock edge arrival variations include, for example, clock frequency fluctuations (jitter) and/or register to register clock edge arrival variations (skew). Both data path and clock edge arrival variations can arise from a number of sources including, for example, ambient chip conditions (e.g., local temperature induced circuit variations or circuit heat sensitivities), power supply noise and chip process variations. In particular, power supply noise can cause clock propagation delay variations through clock distribution buffers. Such clock propagation delay variations can cause skew variations from clock edge arrival time uncertainty at the registers. Typically, chip process variations include device length variations with different device lengths at different points on the same chip. So, a buffer at one end of a chip may be faster than another identical (by design) buffer at the opposite end of the same chip. Especially for clock distribution buffers, these process variations are another source of timing uncertainty.

[0005] Furthermore, as technology features continue to shrink, power bus or V_{dd} noise is becoming the dominant contributor to total timing uncertainty. High speed circuit switching may cause large, narrow current spikes with very rapid rise and fall times, i.e., large dI/dt. In particular, each of those current spikes cause substantial voltage spikes in the on-chip supply voltage, even when power supply inductance (L) is minimized. Because the voltage across the inductor is V=LdI/dt, these supply line spikes also are referred to as L dI/dt noise or, simply, dI/dt noise. Since current switching can vary from cycle to cycle, the resulting noise varies from cycle to cycle. When the V_{dd} noise drops the on-chip supply voltage in response to a large switching event, it slows the entire chip, including both the clock path (clock buffers, local clock blocks, clock gating logic and etc.) as well as the data path logic (combinational logic gates, inverters and etc.) and may cause the chip to fail. When the noise dissipates and the on-chip supply later recovers, or even overshoots as the supply current falls; then, the circuits (buffers, gates and etc.) in these same paths speed up, returning to their nominal performance (with the normal stage delay) or even faster when the supply rises above nominal. If the supply rises too far above nominal, devices may be stressed beyond breaking to damage the chip

or, at the very least reduce chip reliability. The number of stages that can complete changes as the data path slows down or speeds up relative to the clock path. Currently, in particular, such switching noise is a significant component of total timing uncertainty, comparable to skew or jitter (which are themselves affected by switching noise) or chip process variations.

[0006] Thus, it would be useful to be able to identify dI/dt noise as it occurs and minimize how it affects circuit performance.

SUMMARY OF THE INVENTION

[0007] It is a purpose of the invention to improve integrated circuit (IC) chip design;

[0008] It is another purpose of the invention to reduce dI/dt chip effects;

[0009] It is yet another purpose of the invention to simplify chip design requirements for dI/dt effects;

[0010] It is yet another purpose of the invention to sense the onset of dI/dt noise and take steps to minimize how it affects circuit performance.

[0011] The present invention relates to a supply noise compensation circuit. The supply noise compensation circuit senses the onset of dI/dt noise events on a supply line and selectively gates off/forces on a chip clock to chip circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

[0013] Figure 1 shows a block diagram of an example of a supply noise compensation circuit according to a preferred embodiment of the present invention;

[0014] Figure 2 shows dI/dt noise in a supply line;

[0015] Figure 3 shows a noise compensation circuit with a simple voltage sense sensing dI/dt spikes.

DESCRIPTION OF PREFERRED EMBODIMENTS

[0016] Turning now to the drawings and, more particularly, Figure 1 shows a block diagram of an example of a supply noise compensation circuit 100 according to a preferred embodiment of the present invention. A local clock block (LCB) or clock buffer 102 receives and re-drives a global chip clock 104 into 2 complementary local clocks 106, 108. One clock, a launch clock 106, is provided as an input to a delay line 110 that is sensitive to supply voltage changes. The local clock, e.g., launch clock 106, enters the delay line 110 and, as it propagates through the delay line 110, the LCB 102 and delay line 110 mimic data propagation delay through an actual data path, e.g., in a microprocessor. In particular, the launch clock propagating along the delay line 110 reflects propagation delay variations resulting from switching or dI/dt noise on the circuit power supply (V_{dd}) line. Both the launch clock 106 and the second clock, a capture clock 108, clock an N bit register 112. For example, N = 129 may be convenient for holding 3 edges worth of clock edges. The N bit register 112 latches the state of the delay line 110 as reflected at delay line taps 114. Thus, in this example the capture clock 108 captures

the forward position of the timing edges in the N bit register 112. Register contents are interrogated in compare circuit 116, which locates timing edges in the delay line 110 and identifies clock cycle to clock cycle delay changes, up or down. Thus, the delay line and register 112 act as a supply noise sensor. The output of the compare circuit 116 is an input to a clock skip circuit 118, which selectively throttles back on the clock, e.g., selectively skipping one or more clocks.

[0017] Although in this example, the launch clock 106 drives the delay line 110, either clock, the launch or the capture clock, can drive the delay line 110. In this example, the rising edge of launch clock 106 and the falling edge of the capture clock 108 (which latches the data) are coincident, and this edge of interest marks the end/start of the cycle boundary. It should be noted that the present invention is described herein with the registers (e.g., 112) being clocked by complementary clocks 106, 108. This is for example only and not intended as a limitation and the registers/latches may be pulsed latches or any suitable equivalent register/latch such as are well known in the art.

[0018] Preferably, the delay difference between each pair of taps 114 is equivalent to one logic block delay. Typically, the total timing uncertainty metric is the number of combinational logic stages that complete in a cycle, sometimes referred to as the fan-out of 4 (FO4) inverter count or FO4 number. However, for the best time resolution the preferred delay between delay line taps 114 is the minimum delay for the particular technology, e.g., the delay for a single fan-out (FO1) inverter or, for example 20 picoseconds (20ps). Preferably also, the delay line 110 is at least three clock periods long with nominal supply voltage, i.e., long enough that the start of one clock cycle, the leading clock edge, has not propagated through the delay line 110 before the start of second following cycle enters the delay line 110. Therefore, preferably, in the absence of noise the delay line 110 has 3 edges passing through it. The N bit register 112 is clocked by both the launch clock 106 and the capture clock 108. Essentially, at the start of a global clock period, the launch clock 106 passes a previously loaded N bits out of the register 112 as the leading edge begins traversing the delay line 110. At the end of each

global clock period, the capture clock 108 latches the state of the delay line taps 114 in the capture register 112, capturing the progress of the launch clock 106 edges through the delay line 110. The captured edges are at evenly spaced taps 114 in the absence of dI/dt noise other sources of timing uncertainty and such other sources may cause a variation of a couple of taps 114. However, upon the occurrence of dI/dt noise, the edge locations may be much more closely spaced when the supply voltage spikes negative (below V_{dd}) because the delay line is slower and much more widely spaced when the supply is rebounding (above V_{dd}).

[0019] The delay line 110 may be a series of suitably loaded inverters with delay line taps 114 being the inverter outputs, for example. As a result, the taps 114 alternate ones and zeros and the clock edges are located by a matched pair (either 2 zeros in a row, or 2 ones in a row) of adjacent delay line taps 114. The space between matching tap pairs, e.g., 60 inverter stages or 1.2 nanoseconds (1.2ns for 20ps inverters) between leading/rising clock edges for 3 clock edges traversing a 128 tap delay line 110, is a measure of logic propagation during a complete clock cycle. Thus, essentially, the same local clock block 102 both launches and captures the timing edges and, because the local clock itself is the launched data, the clock takes a snapshot of itself in the capturing latches.

[0020] Jitter from a phase locked loop (PLL), for example, may cause as much as a few occasional short cycles in a row. Although not required, the circuit timing can be adjusted so that the first edge (e.g., a leading or rising edge) is always captured in bit position 0 (register latch 0) and in the absence of jitter, the second (leading) edge is in bit 60 and the third in bit position 120. Without clock timing uncertainty, the edges always fall in the same positions, 0, 60, 120. However, with an occasional short cycle the second edge (for the shorter cycle) shifts by one to bit 59; the third edge is captured in bit 119. With 2 consecutive short cycles, however, the second edge still shifts to bit 59, but the third edge shifts to bit 118. In each example, the short clock is no more than a single delay shorter/longer than its neighbors.

[0021] Figure 2 shows an example of a section of a supply noise characterization plot 120 showing dI/dt noise in a supply line, which may be characterized as described in U.S. Application Serial No. _____ (Attorney Docket No. YOR920030363US1) entitled "BUILT IN SELF TEST FOR MEASURING TOTAL TIMING UNCERTAINTY IN A DIGITAL DATA PATH" to Robert L. Franch et al., filed coincident herewith, assigned to the assignee of the present invention and incorporated herein by reference. Upon the occurrence of a dI/dt noise spike, which typically lasts several clock cycles (e.g., anywhere from 10 – 50 cycles), the noise spike drives the supply to the delay line inverters 110 below nominal, reducing inverter switching speed and increasing inverter propagation delay, 2 – 3 register bits at about 2ns in this example 120. By the end of the next cycle at about 3.6ns in this example, the delay line slows such that the preceding edges have propagated 10 fewer stages. Also, it should be noted that the present invention has application to measurement results as described in Franch et al. and such measurements may be used to sense the onset of a dI/dt noise event to mitigate the effects of such an event in accordance with the present invention.

[0022] So for this example, instead of edges being captured at register bit locations 1, 60 and 120, by the end of the first cycle, edges are captured edges are at register bit locations 1, 58 and 116 because the noise spike slows both edges. Further, by the end of the second cycle, captured edges are at register bit locations 1, 50 and 108. Similarly, as the current responsible for the noise spike begins to fall, the supply voltage spikes positive, accelerating edge travel through delay line 110 to the point where only 2 edges (in this example) are propagating through delay line 110. A preferred embodiment integrated circuit (IC) or IC with a supply noise compensation circuit (e.g., 100 in Figure 1) senses the onset of dI/dt noise and responds by selectively skipping/forcing clock cycles to mitigate the dI/dt noise spikes and so, the extreme effects of dI/dt noise spikes.

[0023] So referring again to Figure 1, when the compare 116 identifies at least a 2 bit position reduction between cycles, for example, the compare 116 sends a signal to skip control circuit 118 to block the clock for at least the next cycle. Optionally, in

addition whenever, the compare 116 identifies at least a 2 bit position increase between cycles, for example, the compare 116 sends a signal to skip control circuit 118 to force the clock for at least the next cycle, i.e., preventing clock blocking for at least the next cycle. Furthermore, a single supply noise compensation circuit 100 may be located at the beginning of the chip clock tree, throttling the whole chip down/up in response to dI/dt noise or, supply noise compensation circuits 100 may be distributed throughout the chip clock tree, selectively throttling portions of the chip down/up in response to localized dI/dt noise.

[0024] In particular, for a complex pipelined IC such as a microprocessor, where chip units or block of logic may use localized power up/down techniques, a local supply noise compensation circuit 100 may be provided with the chip units. Each local supply noise compensation circuit 100 may selectively delay powering up/down to better distribute instantaneous chip supply demands and, thereby, reduce dI/dt noise. Also, skip driver 118 may be selected to block/force cycles until the event has subsided partially or completely (e.g., an AND of the output of compare circuit 116 with the global clock), to block/force alternate cycles or any combination thereof.

[0025] Further, a simple voltage sense may be used to sense dI/dt spikes as shown in the noise compensation circuit 130 example of Figure 3, instead of delay line 110 and register 112 of the example 100 of Figure 1. In this example, supply voltage is averaged with in an RC filter 132 and compared in voltage compare 134. A skip timer 136, e.g., a simple D-type latch, is synchronized to global clock 138 and selectively block/passes the global clock in AND gate 138. When the instantaneous supply voltage to voltage compare circuit 134 is below the average voltage at RC filter 132 by a minimum instantaneous voltage difference (d), the voltage compare circuit 134 indicates the occurrence of dI/dt noise. Upon receipt of the indication, the skip timer 136 send a block signal synchronized to global clock 138 to the AND gate 140 that blocks at least the next clock cycle. The skip timer 136 prevents spurious local clocks from occurring, e.g., from a change in the voltage compare 134 mid cycle.

[0026] Thus, advantageously, a preferred embodiment IC can sense the onset of dI/dt noise and avoid the potentially disastrous effects on IC units and even mitigate the dI/dt noise spike itself.

[0027] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.